PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Philip Mattos et al.
Application No.	:	10/632,530
Filed	:	August 1, 2003
For	:	INTEGRATED CIRCUIT FOR CODE ACQUISITION
		Examiner : Ted M. Wang
		Art Unit : 2611
		Docket No. : 851963.410
		Date : March 28, 2007

Mail Stop Amendment
Assistant Commissioner for Patents
Washington, DC 20231

RULE 131 DECLARATION

Assistant Commissioner for Patents:

I, Philip Mattos, residing at Croft Cottage, Newham Bottom, Ruardean Woodside, GL17 9UB, United Kingdom, declare as follows:

1. I am an original, first, and joint inventor with Marco Losi of the subject matter which is claimed and for which a patent is sought for the application identified above.

2. We were in possession of the invention defined by the claims of the application identified above ("the present application") prior to April 4, 2002.

3. The attached invention disclosure form (Exhibit A) was created prior to April 4, 2002 and discusses the invention described in the claims of the present application. I provided this invention disclosure form to the patent department at STMicroelectronics Limited, which is an assignee of the present application, prior to April 4, 2002. I then provided additional disclosure of embodiments of the invention as a Powerpoint document (Exhibit B) to my patent attorney, Mr. Ian Loveless by email also prior to April 4, 2002. Pages 5 and 9 of this Powerpoint document show and describe the embodiments corresponding to Figures 7 and 3 of the present application, respectively.

4. Based on my own personal knowledge, or based on my understanding and belief, each of the dates redacted from Exhibit A is prior to April 4, 2002.

5. Upon my understanding and belief, Mr. Loveless then diligently prepared and filed European Patent Application No. 02255421.6 on August 2, 2002 directed towards the subject matter of my invention disclosure. My understanding is that the present application claims priority based on that European application.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

28th March 2007
Date

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Philip Mattos

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929552

4:33SC Exhibit A page 1/3

From: Ian Loveless
To: jean-jacques.de-jong@st.com
Date:
Subject: Re: Invention 01-IMS-018 from Phillip Mattos

Jean-Jacques

I acknowledge receipt, and will let you have our file number for this proposed European application shortly.

Regards

Ian

>>> <jean-jacques.de-jong@st.com> >>>
Ian,

Here is a new invention disclosure I would like your firm to handle.
We didn't get any other documents from the inventor.

The inventor is a manager, thus hard to get hold of.

JJJ

Forward Header

Subject: Invention 010629-16:51:09 from Phillip Mattos
Author: system (system@crw805.cro.st.com) at internet
Date:

Invention Disclosure Form from Phillip Mattos
Proposal ID: 010629-16:51:09

Instructions: The information contained in this document is COMPANY CONFIDENTIAL and may not be disclosed to others without prior authorization. No patent protection is possible until a patent application has been prepared and submitted to a Patent Office.

Title of Invention:

Using adaptive sampling rate to allow faster GPS acquisition processing but more accurate GPS tracking processing.

Site: Bristol
Group: TPA - Telecom and Peripherals/Automotive
Division and related project: GPS Applications

Category: S - System, anything above circuit level

Product class: BICMOS; CMOS; AUTOMOTIVE; RF; SIGNAL PROCESSING; DESIGN; PROCESSORS;

***Disclosure:

Exhibit A
page 2/3

* Was a description of the invention published, or are you planning to publish one? If so, the date(s) and publication(s):

Not yet

* Was a product including the invention announced, offered for sale, sold, or is such activity proposed? If so, the date(s) and location(s):

Not Yet

* Was the invention disclosed to anyone outside of ST, or will such disclosure occur? If so, provide the date(s) and name(s). Was the disclosure confidential, or will it be?

Yes, to Sige Semiconductor and Sigem, under NDA
Agrate....???
Cambridge

*** Description of Invention

1. Problems solved by the invention.

Acquisition is very compute intensive... the load can be reduced by minimising the sample rate... which must be high during tracking for accuracy. Sensitivity is preserved by combining the information in the samples, not just throwing some away.

2. Prior known solutions and their disadvantages. Why are these insufficient?

3. What was the starting point or main idea which led to the invention?

St20GP1/6/Vespucci GPS dsp, desire for greater sensitivity... which can be achieved in constant time by greater processing power, which in effect is given by this idea, even on the same correlator hardware

4. Advantages (technical and business) of the invention over what has been done before.

more sensitivity in constant time, or faster acquisition in constant hardware processing.

5. Description of the construction and operation of the invention

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*** Inventor Details and Signature

I declare that the invention described in this document was made by me, together with the other inventors listed here, in the course of my normal product development or other duties as an employee of ST. I think that ST should, if it sees fit, file patent applications in its

Exhibit A
page 3/3

name and at its cost. I agree to cooperate fully in any necessary formalities associated with any such patent applications.

If I do not agree that ST may pass upon request information relating to my last registered address to the Patent Attorney, I will let the IP department know by separate mail.

Inventor's Name (LDAP authenticated): Philip Mattos

Home Address:
Croft Cottage, Newham Bottom
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Glos
GL17 9UB

Citizenship: UK

Date of signature:

Email: philip.mattos@st.com
TINA: 065 2541

Witness(es):

Marco.Losi@st.com

List of attachments (if any) that will follow with a hardcopy of this form:

Block diagram

CC: Gisele.PONCET/OU=04/OU=crolles/OU=france@eux100.sgp.st.com

Exhibit B

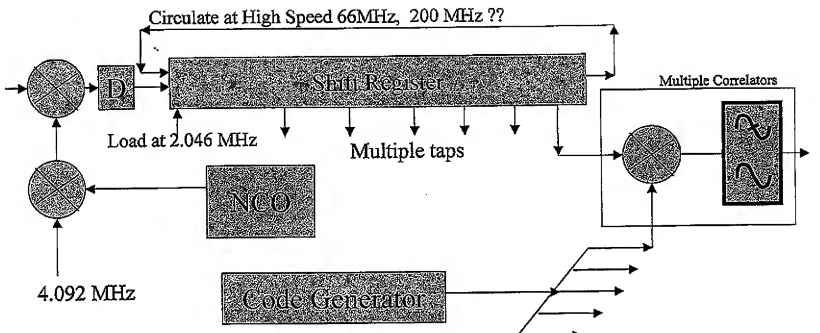
- **GPS = –130dBm …..+ 5dB overspec+5dB antenna –(-170dBm) No = +50dB**
- **Weak satellites, low angles +30dB C/No**

- **Acquire first 41dB, rest 33dB, track 25dB**
- **Buildings about 25dB attenuation**
  - **Very variable.**
  - **Means 25db to 0dB C/No !!!!!**

- **41dB first satellite was set for speed**
- **1ms integration period, 2046 code trials,FFTs, ie 2 seconds real time**
- **Use 12 channels in parallel – 1/6 second**
- **Overheads of satellite maths before, confirmation afterwards. These do NOT extend… only the dsp extends.**

- **Integrate longer**
  - **Slower response**
  - **Narrows bandwidth and 50% benefit….but**
  - **FFT maintains bandwidth and full benefit.**
  - **Integration limited by databit edges**
    - **Predict/synchronise/limit** to 20ms/20+20/~20

- **Add MIPS … but may need i/o b/w**
- **Add correlators… but may need i/o b/w**
  - **ST100/ST120/Sunshine??? Reuse after startup**
- **Add hardware accelerators… FFT / Iqmix**
- **Add full acquisition engine**
- **Combinations of the above**



All signal path repeated for Q channel

D is a decimator, combining groups of 8 samples

Note that existing correlators could be used in a integrated system, subject to fast technology.

BACKGROUND

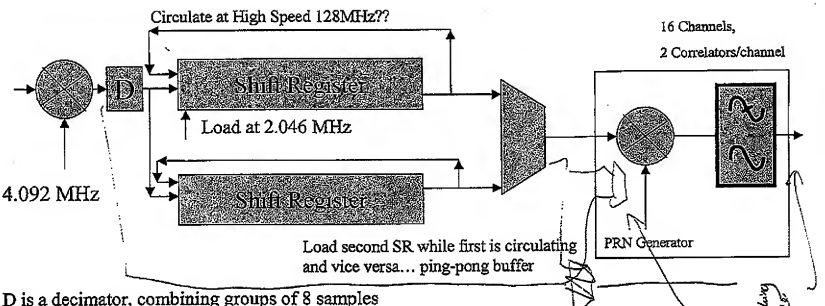
- D is the 16 to 2 MHz sample reduction… /8
- N taps at 66MHz is 4ND times faster than 1 GP6 channel
- ---ND/3 times GP6 12 chans
- ---12 taps 32 times faster
- N taps at 198.208 MHz is 12ND times faster than 1 GP6 channel
- ---ND times GP6 12 chans
- ---12 taps 96 times faster
- Note that 12 taps can be merged with the existing channels, rather than as an acquisition engine

- 32 times faster means 32 times more sensitive at the same acquisition speed (subject to available mips for the longer FFTs
- About 15dB more sensitive
- The snag : I/O bandwidth or signal bandwidth
- no possibility of 200MHz clock
- need 1ms integrations to hold down I/O rate
- thus only cover 1KHz bandwidth....but another 12dB sensitivity gained.
- need 62uS integrations plus h/w convolve or FFT as they will be delivered every 2 microseconds.

- Decimator reduces B/W to 2 MHz....ok
- Existing 62 cycle integrate covers 32KHz only.... Hence front end NCO.....or TCXO
- Existing 62uS integrate is now 500uS, 2KHz
- Existing 31uS integrate is now 250uS, 4KHz
- Existing 1ms integrate is now 8ms, 125 Hz.

High Sensitivity … Hardware acquisition engine…

All signal path repeated for Q channel



D is a decimator, combining groups of 8 samples

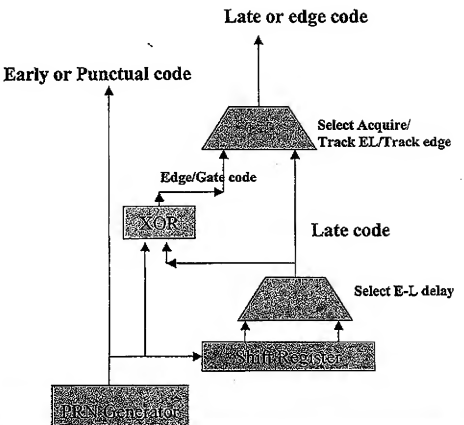
x8 (decimator) x8 (128 versus 16 clock) x2 (correlators/chan) x16 (channels) is x2046 real time.

Therefore hardware can perform all 2046 correlations in 1ms.

Outputs can be stream to memory, software can decide integration time.

Problem… can output side operate fast enough…2046 FFT's every (desired integration time)

Code Generator for dual correlator channel



Truth table			
Input	X	0	1
Code	0	1	1
Action	-	down	up

Text:

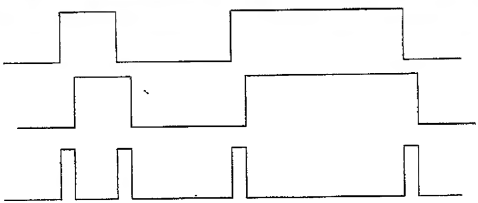
If edge code is 0, do not count.

If edge code is 1,

count up if data = 1,

count down if data = 0

Edge Correlator code generator waveforms



Traditional:

Tracking Error = (sum of (E x Data)) – (sum of (L x Data))

Edge Correlator:

Tracking Error = sum of (data x (E-L))

Benefit : Data is (Signal + 100 Noise) due to –20dB SNR

At 1/16th spacing, 15/16th noise is rejected, no tracking signal rejected.